SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO-1449 FORM	ATTY. DOCKET NO. 10746/23	U.S. SERIAL NO. 09/754,632
	APPLICANT(S) Kazuo Aoyama et al.	
	FILING DATE January 4, 2001	GROUP 2815

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE*
DL	5,256,911	October 26, 1993	Mark A. Holler et al.			
	5,305,250	April 19, 1994	Fathi M. A. Salam et al.			
	4,873,661	October 10, 1989	Yannis Tsividis			
DL	5,343,555	August 30, 1994	Gökce Yayla et al.			

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
DL	WO 99/66419*	December 23, 1999				Abst.*	
DL	EP 1 014 274 A1 ✓	June 28, 2000	Europe			English	
DL	11-194924 ✓	July 21, 1999	Japan			Abst.	

*Corresponds to EP 1 014 274 A1 (English).

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DL	✓	Czezowski, Peter J. et al. "Fuzzy Neurons: A Coarse-Grained Reconfigurable Element for Computational Intelligence"; Electrical and Computer Engineering, 1999 IEEE Canadian Conference on Edmonton, Alta., Canada 9-12 May 1999, Piscataway, NJ, USA, IEEE, US, 9 May 1999, pp. 1074-1080.
DL	✓	Horio, Y. et al. "Switched-Capacitor Chaotic Neuron for Chaotic Neural Networks"; Proceedings of the International Symposium on Circuits and Systems. (ISCS). Chicago, May 3-6, 1993, New York, IEEE, US, vol. 2, 3 May 1993, pp. 1018-1021.
DL	✓	Shibata, Tadashi et al. "FA 15.3: Real-Time Reconfiguration Logic Circuits Using Neuron MOS Transistors"; IEEE International Solid State Circuits Conference, IEEE Inc. New York, US, vol. 36, February 1993, pp. 238-239, 295.

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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DL		7-1 619 42	6/23/95	Japan			X	
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DL	✓	Hiroshi Sawada, et al., "Consideration for a Reconfigurable Logic Device using Neuron MOS Transistor", TECHNICAL REPORT OF IEICE. CPSY99-89, pp. 41-48, Nov. 27, 1999
DL	✓	Kazuo Aoyama,et al., "A Design Method for a Circuit with Neuron MOS Function", TECHNICAL REPORT OF IEICE. CPSY99-90, pp. 49-56, Nov. 27, 1999.
DL	✓	Kazuo Aoyama, et al., "A Method for Designing a Circuit wit Neuron MOS Transistors Realizing any Logic Function", The 13th Workshop on Circuits and Systems in Karuizawa, pp. 113-118, April 24-25, 2000.

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DL	✓		Tadashi SHIbata, et al., "A Functional MDS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 39, No. 6, pp. 1444-1455, June 1992.
DL	✓		~~Tadashi Shibata, et al., "Real Time Reconfigurable Logic~~ Circuits Using Neuron MOS Transistors", International Solid-State Circuits Conference, 1993.
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DL	✓		S.D. Brown, et al., "Field-Programmable Gate Arrays", Kluwer Academic Publishers

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DL	5 990 709	November 23, 1999	Thewes, et al.			

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DL	0 566 739 ✓	October 27, 1993	Europe				
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DL	✓	Tadashi, Shibata, et al. "Neuron MOS Voltage-Mode Circuit Technology for Multiple-Valued Logic" IEICE Transactions on Electronics, Institute of Electronics Information and Comm. Eng. Tokyo, JP, vol. E76-C, no.3, 1 March 1993, pp. 347-356.

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